UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/692,024	10/23/2003	Ralf Staub	INF 2003-US/PC	8527

46798 7590 07/12/2005

MOSER, PATTERSON & SHERIDAN, LLP
GERO G. MCCLELLAN/INFINEON
3040 POST OAK BLVD.,
SUITE 1500
HOUSTON, TX 77056

EXAMINER	
ESTRADA, MICHELLE	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 07/12/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/692,024	STAUB ET AL.	
	Examiner	Art Unit	
	Michelle Estrada	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *11 and 14-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *11 and 14-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15, 17 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Lu (6,218,693).

Re claim 11, Lu discloses a trench capacitor (32/34); and a select transistor (14/16/18), comprising: a diffusion region forming a source/drain (17/19) electrode of the select transistor (Col. 3, lines 30-62); a bit line contact (30') formed in an insulator layer (20) and comprising a filling comprising a metal alloy (Col. 2, lines 34-41), wherein the bit line contact connects the source/drain region to an associated bit line (30) (See Fig. 4); and a doped region (19) formed in the source/drain electrode to contact (Col. 2, lines 12-14) the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact.

Re claim 14, Lu discloses wherein the select transistor (14/16/18) is at least partially disposed in the substrate and the trench capacitor is completely disposed in the semiconductor substrate (10) (See Fig. 4).

Re claim 15, Lu discloses wherein the bit-line contact comprises at least one or tungsten, aluminum and copper (Col. 2, lines 34-41).

Re claim 17, Lu discloses wherein the bit-line contact further comprises a liner (barrier) layer formed between the substrate and the filling of the bit-line contact (Col. 2, lines 34-41).

Re claim 18, Lu discloses wherein the liner layer comprises Ti/TiN (Col. 2, lines 34-41).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lu as applied to claims 1-15, 17 and 18 above, and further in view of Dennison et al. (6,429,069).

Lu does not disclose wherein the memory cell is part of a memory cell arrangement comprising peripheral contacts that are formed in a same structure plane and comprising a filling substantially similar to that of the bit-line contact.

Dennison et al. disclose a memory cell arrangement comprising peripheral contacts (50/54/56) that are formed in a same structure plane and comprising a filling substantially similar to that of the bit-line contact (48) (Col. 6, line 66-Col. 7, line 1 and Fig. 4B).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Lu and Dennison et al. to enable the peripheral contacts formation step of Dennison et al. to be performed in the process of Lu because by making the peripheral contacts and the bit-line contact on the same structure plane and of the similar material, all of them can be made in a single step saving process steps, time and manufacturing costs.

Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lu as applied to claims 1-15, 17 and 18 above, and further in view of Bollinger et al. (6,762,136).

Re claim 19, Lu does not disclose an annealed region formed as a result of an anneal process performed during fabrication of the bit-line contact.

Bollinger et al. disclose an annealed region formed in the silicon substrate after implantation of the doping material (Col. 2, lines 10-14).

It would have been within the scope of one of ordinary skill in the art to combine the teachings of Lu and Bollinger et al. to enable the annealed region formation step of Bollinger et al. to be performed in the process of Lu because the annealing will repair the crystal damage done by the implant process in the bit-line contact (Col. 2, lines 13-14).

Re claim 20, Bollinger et al. discloses wherein the annealed region includes a damage region damaged during a doping processed performed to form the doped region (Col. 2, lines 10-15).

Re claim 21, Bollinger et al. disclose wherein the annealed region includes at least a portion of the doped region (Col. 2, lines 10-15).

Re claim 22, Lu discloses wherein the bit-line contact further comprises a liner (barrier) layer formed between the substrate and the filling of the bit-line contact (Col. 2, lines 34-41).

Re claim 23, Lu discloses wherein the liner layer comprises Ti/TiN (Col 2, lines 35-37).

Re claim 24, Lu discloses wherein another source/drain electrode (17) of the select transistor is connected to an electrode (34) of the trench capacitor, which is completely disposed in the substrate (See Fig. 4 and Col. 3, lines 55-58).

Response to Arguments

Applicant's arguments filed 5/3/05 have been fully considered but they are not persuasive. Applicant argues that Lu does not disclose a doped region formed in the source/drain electrode to contact the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact. And further points out that the conductive layer of Lu projects underneath the insulating layer adjoining the bit line contact. However, Lu discloses a doped region (19) formed in the source/drain electrode to contact (Col. 2, lines 12-14) the filling of the bit-line contact, the doped region comprising a locally limited electrically conductive contact layer which is formed underneath the bit-line contact in the diffusion region and which has a relatively reduced lateral migration underneath the insulator layer adjoining the bit-line contact as explained in the rejection under 35 USC 102. Also, the conductive layer of Lu is formed underneath the bit-line contact in the diffusion region as shown in Fig. 4. If Applicant intends to claim that the conductive layer does not projects underneath the insulating layer adjoining the bit line contact, it must be clearly recited. The reference still encompasses the language of claims 11 and 19, which recites that the conductive contact "has a relative reduced lateral migration underneath the insulator layer adjoining the bit-line contact".

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michelle Estrada whose telephone number is 571-272-1858. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on 571-272-1907. The fax phone numbers for the organization where this application or proceeding is assigned are 571-273-0224 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2800.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Michelle Estrada
Patent Examiner
Art Unit 2823

ME
June 28, 2005